REMARKS/ARGUMENTS

Reconsideration and allowance are respectfully requested. No new matter has been added by the amendments herein.

Claim Rejections

Claims 1, 3-9, 11, and 13-15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,781,799 to Leger, et al. ("Leger") in view of U.S. publication no. 2003/0033454 A1 to Walker et al. ("Walker"), and further in view of U.S. Patent No. 6,870,929 to Greene ("Greene"). Applicant respectfully traverses this rejection.

Independent Claim 1

Leger

Independent claim 1 recites:

> coupling said respective DMA modules over a data transfer facility in a chain arrangement where each DMA module, other than the last in the chain, has its respective output buffers coupled to the input buffer of another of said DMA modules downstream in the chain and each of said DMA modules, other than the first in the chain, has its respective input buffer coupled to the output buffer of another of said DMA modules upstream in the chain….

and further recites:

> when said reading of data from the respective IP block into the output buffer of the DMA module is completed, the data in the output buffer of the DMA module are transferred to the input buffer of the DMA module downstream in the chain or, in the case of the last DMA module in the chain, are provided as output data….

The Office Action compares the recited DMA modules with DMA controllers 20 of Leger (Fig. 2), alleging that the DMA controllers 20 are connected in a daisy chain. However, as conceded by the Office Action, Leger fails to teach or suggest (1) coupling input and output

buffers of DMA modules in a chain, and (2) transferring the recited data from the output buffer of one DMA to the input buffer of another DMA, as recited in claim 1.

Leger plus Walker

Instead, the Office Action alleges that it would have been obvious to modify Leger to incorporate input and output buffers that are allegedly part of the multi-port DMA 5 of Walker (Fig. 2) into each of the DMA controllers 20 of Leger, so as to facilitate coupling between DMA modules. The alleged motivation for modifying Leger would be to enable other modules to access the system bus while a DMA controller is handling a transfer between two modules (referring to Walker at paragraph 5, lines 2-6).

However, Walker at paragraph 5 is not concerned with transferring data between two DMA controllers, as alleged by the Office Action, but rather discusses the problems that arise when a DMA controller handles a transfer between two "modules," or locations. See also Walker paragraphs 0009 and 0011, which discuss how a DMA controller can perform a data transfer between two locations, such as a processor, memory, or bus, without occupying the system bus. In this case, there is nothing to teach or suggest that the two modules, or locations, are two DMA controllers that are communicating with each other. In fact, Walker does not even teach or suggest using more than one DMA controller.

The Office Action responds to the above argument by stating that "the coupling of DMA ports as shown in Walker *could* be used to ensure the transfer of data between said ports, which could be interpreted as modules." Office Action, numbered paragraph 13 (italics added). Applicant respectfully disagrees, for the following reasons.

First, while Walker does disclose connecting any of ports A, B, C, and D together, these ports are all part of the same DMA controller. Thus, this never teaches or suggests connecting different DMA controllers together. When combined with Walker, Leger at best teaches using a multi-port DMA controller in which the controller's ports are connected together.

Second, it is respectfully submitted that the above-quoted response in the Office Action is mere speculation, without support from Walker or any other source. The reasoning of the Office Action implies the absurd conclusion that anything *could* be connected to anything else. In fact, Walker does not teach or suggest connecting the ports of the DMA controller to anything other

than (1) other ports of that same DMA controller, or (2) other types of modules. There is nothing in Walker to teach, suggest, or even imply chaining together multiple DMA controllers, or that the other modules could be other DMA controllers. Walker does not envision a need for multiple DMA controllers.

Thus, even if Leger were somehow modified with the buffers of Walker as proposed, this still would not result in a system where two DMA controllers are coupled together in the manner claimed.

Applicant further respectfully disagrees with the stated reasoning for modifying Leger with Walker. The Office Action states that it would have been obvious to modify Leger with Walker "because the addition of an input buffer and an output buffer can facilitate coupling between two DMA modules." This is a circular argument. As previously explained, Walker does not teach or suggest coupling a port of the DMA module with another DMA module; there is no other DMA module in Walker. Thus, the resulting modified Leger/Walker system still would not couple the ports of multiple DMA modules together.

The Office Action goes on to state that the motivation for modifying Leger with Walker "would have been to mitigate the typical disadvantage of conventional DMA controllers, wherein said conventional DMA controller acquires complete control of a bus." But this alleged motivation is taken from Walker, which again, does not teach or suggest coupling multiple DMA controllers together. Thus, this alleged reasoning does not explain why or how one would arrive at DMA modules coupled together as claimed. In fact, Walker alleges being capable of mitigating the bus control issue with only a single DMA controller.

Leger plus Walker, plus Greene

The Office Action further relies on Greene for the feature of the DMA modules being coupled in a chain as recited. Greene uses a plurality of cipher stages 802 arranged in a pipeline to perform data encryption. Each cipher stage 802 includes a combinational section 804 and a pipeline register 806 (see Fig. 8). The Office Action alleges that it would have been obvious to modify the data-exchanging method of Leger/Walker to include the combinational sections and pipeline registers of Greene, because the chain of such combinational sections and pipeline registers would enhance the overall performance of the data processing transfer. The alleged

motivation would be to prevent delays and unnecessary idle times (referring to col. 4, lines 2-4 of Greene).

In other words, it appears that the Office Action proposes to add the encryption function of Greene to the Leger/Walker system.

Applicant respectfully submits that, even though DMA and encryption functions both involve the processing of data, one cannot simply transplant the various encryption elements from the Greene encryption system into the Leger/Walker DMA system and expect it to work. Moreover, the Office Action has not cited any valid reason why one would have wanted to add encryption to a DMA system in the first place.

The Office Action's allegation that the modification would have prevented delays and unnecessary idle times does not apply here. The col. 4, lines 2-4 statement of Greene is not applicable to the system of Greene Fig. 8, because the statement refers to conventional systems (the statement is located in the Background section of Greene). Moreover, even if this statement were taken as an implication that the Fig. 8 system is faster than conventional encryption systems, there is nothing in Greene to indicate that the specific elements 802, 804, 806 are the ones responsible for making it faster, and that these alone would be sufficient for making a system faster.

Furthermore, and perhaps more importantly, the addition of the encryption elements of Greene to the Leger/Walker system would, if anything have the opposite effect as alleged by the Office Action. In fact, if the combined system worked at all, the addition of an encryption function to the DMA must surely be *slower* than the pure DMA function alone. Therefore, it is respectfully submitted that the alleged reasoning for modifying Walker/Leger with Greene – to speed up the Walker/Leger system – is flawed.

Conclusion

For at least these reasons, it is submitted that claim 1 is allowable over Leger, Walker, and Greene, either alone or in combination.

Independent Claims 5 and 11

Independent claims 5 and 11 are also allowable over Leger, Walker, and Greene for at least similar reasons as discussed above with regard to claim 1.

Dependent Claims

The dependent claims are also allowable by virtue of depending from allowable independent claims, and further in view of the additional features recited therein.

Conclusion

All rejections having been addressed, Applicant respectfully submits that the present application is in condition for allowance, and respectfully solicits prompt notification of the same. Should the Examiner have any questions, the Examiner is invited to contact the undersigned at the number below.

Respectfully submitted,

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Dated: June 10, 2010

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